In the Specification:

Please replace the paragraph beginning on page 6, line 12 with the following amended paragraph:

FIG. 2 is a schematic diagram illustrating the chip architecture for testing integrated circuit chip **100**. In FIG. 2, integrated circuit chip **100** includes a multiplicity of macro-circuits **150** and a multiplicity of isolation circuits **155**. There is one isolation circuit **155** for each macro-circuit **150**. Each macro circuit **150**/isolation circuit **155** is coupled to a macro-circuit scan multiplexer and control logic **160** by a corresponding bus **165**. Each bus **165** includes wires for at least macro-circuit scan-out signals and isolation circuit scan-in, scan-out and control signals. Macro-circuit scan multiplexer and control logic **160** is further coupled to all the NPG circuit scan chains **170** by a bus **175**. Bus **175** includes wires for at least multiple NPG scan-in signals and multiple NPG scan-out signals. Macro-circuit scan multiplexer and control logic **160** is also coupled to multiple I/O pads **180A** by bus **185A** for receiving scan-in signals from off chip, multiple I/O pads **180B** by bus **185B** for sending scan-out signals off chip and multiple I/O pads **180C** by bus **185C** for receiving mode and configuration control signals from a tester. Mode and configuration control signals are used by macro-circuit scan multiplexer and control logic **160** to configure scan chains for testing either macro-circuits **150** or the NPG circuits of integrated circuit chip **100** as illustrated in FIGs. 3A, 3B, 3C and 4 and described *infra*. While not necessarily separate signals, mode control can be thought of as selecting whether to test macro-circuits or NPG circuits and configuration signals can be thought of as selecting groups of macro-circuits to test together. While isolation circuits **155** are illustrated "outside" of macro-circuits **150**, the isolation circuits may be incorporated within each macro-circuit.